DAVID C. ZARETSKY, PH.D.

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PROFESSIONAL PROFILE

- Innovative entrepreneurial executive with strong leadership and experience in all aspects of business growth: technology, fundraising, business development, sales, marketing, project development, and personnel management.
- Accomplished technology advisor, researcher, engineer, and published author with 20+ years of professional and academic expertise in the fields of IT, data analytics, data science, high-performance computing, and electronic design automation.
- Adjunct Professor & committed educator at top-10 university, with proven track record in developing courses and teaching methods that promote stimulating learning environments across multiple disciplines in engineering and entrepreneurship.

PROFESSIONAL EXPERIENCE

Chief Executive Officer, Chief Scientist, and Co-founder, *Snips Media.* – Chicago, IL 2013–present
- Chief architect of the Snips influencer management platform, real-time analytics, sale tracking, and monetization platform.
- Built strategic partnerships with advertising agencies, brands, media companies, celebrities, and blogger networks.
- Developed business plan, strategic vision, product roadmap, and Series A fundraising initiatives.
- Managed technology, sales, and marketing teams to facilitate company growth in key industry sectors.

President, Chief Executive Officer, Co-founder, *QuickStream.* – Chicago, IL 2011–2015
- Hardware/software design consultant and project manager.
- Managed software product development, both onshore and offshore teams.

President, Chief Executive Officer, Co-founder, *Binachip, Inc.* – Chicago, IL 2007–2011
- Developed business plan, strategic vision, product roadmap, and new revenue streams.
- Managed day-to-day operations, including technology, IT, sales, marketing, and customer relations.
- Principal investigator for 6 SBIR/STTR contracts, generating $1.5M+ in revenue between 2007-2010.
- Chief architect of the company's ESLERATE high-level synthesis product suite.

Director of Engineering and Product Development*, Nastec, Inc.* – Cleveland, OH 2004–2012
- Project manager and chief product engineer of Nastec's aircraft engine and transmission life-monitoring AI system.
- Principal Investigator on 3 NASA SBIR contracts, generating $1.3M+ in revenue.

DSP Engineer, *Xilinx Research Labs* – Longmont, CO 2004
- Developed and optimized MPEG4 and H.264 Video Codecs on Xilinx FPGAs.
- Analyzed first-generation Xilinx Forge (C-to-HDL) high-level synthesis tool and framework.

Corporate Software Engineer, *AccelChip, Inc.* – Schaumburg, IL 2001– 2002
- Front-end multi-platform UI for AccelFPGA EDA software tool.
- Developed key hardware optimizations to improve throughput performance and resource utilization.

Advanced Technology Engineer, *Case-New Holland, Inc.* – Burr Ridge, IL 2000
- Responsible for integrating and optimizing AI, computer vision and GPS navigation into autonomous tractors.
- Developed onboard GUI interface for mapping paths, navigation and controls in autonomous tractors.

PROFESSIONAL LEADERSHIP

- **DePaul University, Coleman Entrepreneurship Center** – Startup Mentor
- **Mentor**, Founders Institute
- **Advisory Board**, Various Startups
- **Director,** America-Israel Chamber of Commerce
- **Member,** Illinois Technology Association

TEACHING

NORTHWESTERN UNIVERSITY
- **Assistant Chair & Associate Professor,** Department of Electrical & Computer Engineering 2015-Present
- **Adjunct Professor,** Farley Center for Entrepreneurship & Innovation 2019-Present

DEPAUL UNIVERSITY
- **Adjunct Lecturer,** College of Computing & Digital Media 2017-Present

EDUCATION & RESEARCH

UNIVERSITY OF ILLINOIS

- **Adjunct Researcher,** Department of Electrical and Computer Engineering 2007-2010
- **Post-Doctoral Researcher,** Department of Electrical and Computer Engineering 2006-2007

NORTHWESTERN UNIVERSITY

- **Post-Doctoral Researcher,** Department of Electrical and Computer Engineering 2005-2006
- **Ph.D. in Electrical and Computer Engineering** 2002-2005
  - Specialization: High-Level Synthesis, Compilers, Binary Translation, SoC FPGAs, and VLSI.
  - Dissertation Title: "A Methodology for Translating Scheduled Software Binaries onto FPGAs"
- **M.S. in Electrical and Computer Engineering** 2000-2001
  - Research: Compilers, High-Level Synthesis, and Parallel and Distributed Computing.
  - Dissertation Title: "Design and Evaluation of Matlab Functions on FPGAs"
- **B.S. in Electrical Engineering / B.S. in Computer Engineering** 1996-2000
  - Earned dual B.S. degrees in Electrical and Computer Engineering.
  - Specialization: Computer Systems Design, Robotics, and Parallel and Distributed Computing.

JERUSALEM COLLEGE OF TECHNOLOGY

- **Study Abroad Program:** Religion, Business Ethics, and Medical/Science Ethics. 1995-1996

SKILLS

Engineering Expertise:

- Artificial Intelligence
- Machine Learning
- Computer Vision
- Data Mining
- Databases
- Ad Technology
- Analytics
- Electronic Design Automation
- High Performance Computing
- Embedded Systems
- Operating Systems
- Compilers
- Digital Signal Processing
- Communication Systems
- High-frequency Trading
- FPGA / ASIC Design
- Microprocessors
- Information Technology
- Cloud Computing
- Machine Learning
- Software Defined Radios

Programming Languages:

- C/C++
- C# / .Net
- Java
- VHDL
- Verilog
- System-Verilog
- Matlab
- JavaScript
- HTML
- PHP
- Python
- Ruby
- Perl
- MySQL
- Binary/Assembly

Spoken Languages:

- English, Fluent
- Portuguese, Fluent
- Hebrew, Fluent

RESEARCH AND SMALL BUSINESS GRANTS

Reputable principal investigator for 9 SBIR and STTR government contracts, totaling over $3 million:

- NASA SBIR II for $600,000, "Aircraft Engine Life-Consumption Monitor for Real-Time Reliability Determination," 2011.
- NASA SBIR I for $100,00, "Aircraft Engine Life-Consumption Monitoring for Real-Time Reliability Determination", 2010.
- NASA SBIR II for $600,000, "In-Service Aircraft Transmission Life Modeling for Improved Flight Safety", 2009.
- ARMY SBIR I for $70,000, "Low Power FPGA Design Tools Using High Level Synthesis," 2010.
- DARPA SBIR II for $750,000, "A High-Level Synthesis Tool for FPGA Design Using Software Binaries," 2009-2011.
- DARPA SBIR I for $100,000, "A High-Level Synthesis Tool for FPGA Design Using Software Binaries," 2007.
- NASA SBIR II for $600,000, "HW/SW Design Environment for Reconfigurable Communication Systems," 2007-2008.
- NSF STTR I for $100,000, "Automated Design Environment for Embedded Systems," 2006.
- NASA STTR I for $100,000, "A System Level Tool for Reconfigurable Hardware," 2005.

SELECTED PUBLICATIONS

- D. Zaretsky, G. Mittal, L. Gao, and P. Banerjee, "A Tool for the Automated Generation of Streaming SoCs," DAC, San Diego, CA, 2011.
- L. Gao, G. Mittal, D. Zaretsky, and P. Banerjee, "Resource Optimization and Deadlock Prevention while Generating Streaming Architectures from Ordinary Programs," AHS, San Diego, CA, 2011.
- L. Gao, D. Zaretsky, G. Mittal, D. Schonfeld, and P. Banerjee, "Automatic Generation of Stream Descriptors for Streaming Architectures," ICPP, San Diego, CA, 2010.

- L. Gao, G. Mittal, D. Zaretsky, D. Schonfeld, and P. Banerjee, "An Automated Algorithm to Generate Stream Programs," ISCAS, Taipei, Taiwan, 2009.
- L. Gao, G. Mittal, D. Zaretsky, D. Schonfeld, and P. Banerjee, "Automatically Generating Streaming Architectures from Ordinary Programs," IASTED PDCS, Cambridge, MA, 2009.
- D. Zaretsky, G. Mittal, and P. Banerjee, "Streaming Implementation of the ZLIB Decoder Algorithm on an FPGA," ISCAS, Taipei, Taiwan, 2009.
- G. Mittal, D. Zaretsky, and P. Banerjee, "Streaming Implementation of a Sequential Decompression Algorithm on an FPGA," International Symposium on FPGAs, Monterey, CA, 2009.
- L. Gao, D. Zaretsky, G. Mittal, D. Schonfeld, and P. Banerjee, "A Software Pipelining Algorithm in High-Level Synthesis for FPGA Architectures," ISQED, San Jose, CA 2009.
- G. Mittal, D. Zaretsky, X. Tang, and P. Banerjee, "An Overview of A Compiler For Mapping Software Binaries To Hardware," IEEE TVLSI, Piscataway, NJ, 2007.
- D. Zaretsky, G. Mittal, R. Dick, and P. Banerjee, "Balanced Scheduling and Operation Chaining in High-Level Synthesis for FPGA Designs," ISQED, San Jose, CA, 2007.
- D. Zaretsky, G. Mittal, R. Dick, and P. Banerjee, "Dynamic Template Generation for Resource Sharing in Control and Data Flow Graphs," VLSI, Hyderabad, India, 2006.
- D. Zaretsky, G. Mittal, R. Dick, and P. Banerjee, "Generation of Control and Data Flow Graphs from Scheduled and Pipelined Assembly Code," LCPC, Hawthorne, NY, 2005.
- G. Mittal, D. Zaretsky, G. Memik, and P. Banerjee, "Automatic Extraction of Function Bodies from Software Binaries," ASP-DAC, Beijing, China, 2005.
- G. Mittal, D. Zaretsky, P. Banerjee, "Tool-flow For an Automated Compilation of Simulink and Real-Time Workshop Applications onto Heterogeneous Platforms," GSPx, Santa Clara, CA, 2005.
- D. Zaretsky, G. Mittal, X. Tang, and P. Banerjee, "Evaluation of Scheduling and Allocation Algorithms While Mapping Assembly Code onto FPGAs," GLSVLSI, Boston, MA, 2004.
- D. Zaretsky, G. Mittal, X. Tang, and P. Banerjee, "Overview of the FREEDOM Compiler for Mapping DSP Software to FPGAs," FCCM, Napa, CA, 2004.
- G. Mittal, D. Zaretsky, X. Tang, and P. Banerjee, "Automatic Translation of Software Binaries onto FPGAs," DAC, San Diego, CA, 2004.
- P. Banerjee, M. Haldar, A. Nayak, V. Kim, V. Saxena, S. Parkes, D. Bagchi, S. Pal, N. Tripathi, D. Zaretsky, R. Anderson, J. R. Uribe. "Overview of a Compiler for Synthesizing MATLAB Programs onto FPGAs," TVLSI, Piscataway, NJ, 2004.
- P. Banerjee, N. Shenoy, A. Choudhary, S. Hauck, M. Haldar, P. Joisha, A. Jones, A. Kanhare, A. Nayak, S. Periyacheri, M. Walkden, and D. Zaretsky. "A MATLAB Compiler for Distributed Heterogeneous Reconfigurable Computing Systems," FCCM, Napa Valley, CA, April 2000.
- S. Periyacheri, A. Jones, A. Nayak, D. Zaretsky, P. Banerjee, N. Shenoy, A. Choudhary. "Library Functions in Reconfigurable Hardware for Matrix and Signal Processing Operations in MATLAB," IASTED PDCS 1999, Cambridge, MA, Nov 1999.

HONORS & AWARDS

- U.S. Patent 7,565,631 B1, "Method and system for translating software binaries and assembly code onto hardware", Jul 2004.
- Chick Evans Scholarship recipient – full 4-year academic tuition scholarship at Northwestern University, 1996-2000.

INTERESTS

- Multi-instrumentalist with 25+ years experience playing guitar, piano, bass, and voice.
- Lindy Hop, Swing, and Blues dancer.
- Avid distance runner and cyclist.

REFERENCES

Available upon request.