Carolyn R. Duran

Curriculum Vitae

Vice President, Memory and IO Technologies
Intel Corporation, Hillsboro, OR 97124
Mobile: (503)702-4716
Email: carolyn.r.duran@intel.com

Education

Ph.D., Materials Science and Engineering, Northwestern University, 1998.

B.S., Materials Science and Engineering, Carnegie Mellon University, 1992.

Professional Experience

Apr 1998 – Present: Intel Corporation, Hillsboro, OR

Vice President and Engineering Manager, Memory and IO Technologies (July 2017 – present)

- Leads a team of >80 experienced engineers, architects and technologists responsible for a wide portfolio of Memory and IO technologies, driving technologies internally and externally through industry standards.
- Intel-wide charter covers strategy, architecture, standardization, validation and ecosystem enabling.

Senior Director, Supply Chain Sustainability (Jan 2010 – Jun 2017)

- Led Intel's overall leadership position supply chain sustainability strategy to meet both regulatory requirements and corporate commitments.
    - Set strategic direction to align resources to areas where we can affect the most change in the supply chain, supplier environmental practices and human rights.
    - Chemical responsibilities not only included supplier compliance to regulations in each geography Intel operates, but also sensing and addressing future potential regulations to mitigate risk to technology development and implementation. Technical advisor on chemical regulatory issues in the supply line, including representing Intel with the EPA, EU, and China MEP. Testified on behalf of downstream scientific users of helium in the Senate Subcommittee for Energy and Natural Resources in May 2013. Testified on behalf of Intel in the House Subcommittee for Energy on Commerce in March 2014 panel on TSCA reform.
    - Primary technical expert and external spokesperson for Intel's Conflict Minerals Program. Led worldwide program to deliver the first conflict-free microprocessors to market. Received an Intel Achievement Award for this work in 2014.

Lithography Commodity Area Manager (Feb 2014 – June 2017)

- Led a team of technologists responsible for developing and implementing leading edge lithography and thin film materials to enable Intel's patterning roadmap; responsible for a commodity management team negotiating contracts with a combined value >$1B.
- Provided commodity support for our global high-volume factory network addressing cost, quality and availability needs throughout the technology lifecycle.

Fab Materials Ramp Program Manager (Jul 2007 - May 2015)

- Ensured all chemicals used within Intel's global manufacturing facilities meet cost, quality, availability, and technical requirements within the supply chain.

Technology Development (Apr 1998 – Jul 2007)

- Wafer level test development Manager
    - Managed a team of experienced engineers and technicians supporting process development for Intel's logic and chipset future technologies. Set strategic and tactical objectives for the area.

    - Led technology development for three concurrent process technologies, and ensured that technical gaps were identified and closed, resources were allocated at the right level, and projects were prioritized to maximize efficiency without jeopardizing quality.
- Thin films Area Manager, Storage Technologies Group
    - Reset and executed a materials selection strategy to demonstrate material capability and drive timely program decisions.
    - Led a team of >25 experienced engineers and technicians supporting thin film process development for an advanced memory program. Managed thin film equipment operations.
    - Provided technical expertise to solve complex problems in both fundamental materials science (metals, metal oxides and metal nitrides) and process integration.
- Process Engineer, Components Research/Portland Technology Development
    - Responsible for process development, new equipment selection and qualification, and sustaining module operations for the copper barrier/seed process, including driving innovative research projects with external suppliers across multiple functional areas.
    - Developed advanced copper and barrier material processes for three generations of interconnect technologies, including a novel solution to meet 90nm design rules for electromigration resistance.

Sep 1993 – Mar 1998, Research Assistant, Materials Science and Eng. Northwestern University Evanston, IL

Feb 1993 – Sep 1993, Process Engineer, Pennsylvania Metallurgical, Inc, Bethlehem, PA

Jan – May 1991, Aug – Dec 1991, May – Aug 1992, Co-op Student, GE Aircraft Engines, Evendale, OH

Awards, Honors and Recognition

- 2016: Fast Company's "Most Creative People in Business 1000"
- 2014: #2, Business Insider's "Most Powerful Women Engineers in the World"
- 2014: Intel Achievement Award
- 1994: National Science Foundation Fellowship
- 1993: Northwestern University Graduate School University Fellowship

Board and Community Service

- 2020: Materials Research Society, 2022 President-elect
- 2016-2017: Board of Directors, Responsible Business Alliance (Chair, 2017)
- 2015-2016: Steering Committee Chair, Responsible Minerals Initiative
- 2009-2015, 2016-2020: Materials Research Society, Government Affairs Committee
- 2005-2017: Board of Directors, Relay Resources, Portland, OR. Held multiple leadership positions on the board including Chair, Vice Chair, and committee leads
- 2008-Present: Northwestern University Materials Science and Engineering Academic Advisory Board
- 2003-Present: University of California Berkeley Materials Science and Engineering Advisory Board
- 2008-2010, 2017-2019: Carnegie Mellon University Materials Science and Engineering Academic Advisory Board
- 2007-2009: University of Michigan Materials Science and Engineering External Advisory Board
- 2008-2014: ABET Program Evaluator, Materials Science and Engineering
- 2004-2006: Dean's Leadership Council, Carnegie Institute of Technology, Carnegie Mellon University
- 2003-2004: Semiconductor Research Corporation Industrial Liaison, High K Dielectrics
- 2000-2001: IITC external reviewer for Interconnect Metallization Paper submissions

Patents

1. Diana, D.C., *Duran, C.R.*, Lindstedt, R.C., Silberstein, M.E. 2008 Ferroelectric polymer memory structure and method therefor, *US Patent Number 7344897*

2. Miaz, J.A., Morrow, X., Marieb, T., *Block, C. (née Duran)*, Leu, J., McGregor, P., Kuhn, M., Taylor, M. 2004 Surface alteration of metal interconnect in integrated circuits for electromigration and adhesion improvement, *US Patent Number 6794755*
3. Marieb, T.N., McGregor, P., *Block, C. (née Duran)*, Jin, S. 2007 Copper alloys for interconnections having improved electromigration characteristics and methods of making same, *US Patent Number 7220674*
4. Marieb, T.N., McGregor, P., *Block, C. (née Duran),* Jin, S. 2005 Copper alloys for interconnections having improved electromigration characteristics and methods of making same, *US Patent Number 6977220*
5. Marieb, T.N., McGregor, P., *Block, C. (née Duran)*, Jin, S. 2004 Copper alloys for interconnections having improved electromigration characteristics and methods of making same, *US Patent Number 6800554*

Speaking Engagements: Supply Chain, Chemicals, Responsible Sourcing

- 2014: Expert testimony, Hearing before the House Committee on Energy and Commerce, Subcommittee on Environment and the Economy. Subject: discussion draft of the Chemicals in Commerce Act.
- 2013: Expert testimony, Hearing before the Committee on Energy and Natural Resources, United States Senate. Subject: Helium Stewardship Act of 2013.

- 2017: Invited Speaker, MMTA International Minor Metals Conference, Dublin. "Delivering a conflict-free supply chain"
- 2017: Speaker, Materials Research Society Symposium ES10: Materials Efficiency to Enable A Circular Materials Economy. "Challenges in Sustainable Sourcing – Intel's Journey"
- 2017: Panelist, 11th ICGLR-OECD-UN GoE Forum on Responsible Mineral Supply Chains, OECD, Paris "Responsible Mining for peace, stability, and development"
- 2016: Keynote, John E. Hilliard Symposium, Materials Science and Engineering, Northwestern University. "Redefining What we Mean by a Quality Product"
- 2016: Panelist, LBMA/LPPM Precious Metals Conference, Singapore, "Session 8: Responsible Gold Guidance"
- 2015: Invited Speaker, Global Philanthropy Forum, Washington DC.
- 2014: Panelist, The Economist Innovation Forum, Berkeley.
- 2013: Invited Speaker, ITRI Tin Forum, Bangka Island, Indonesia.
- 2013: Panelist, LBMA/LPPM Precious Metals Conference, Rome, "Session C: Industry Initiatives"
- 2019: Guest lecturer, Chemical Engineering Graduate Seminar, Brigham Young University. "Conflict Free Microprocessor Materials"
- 2016: Guest Lecturer, Graduate Liberal Studies, Security and Development, Georgetown University.
- 2014: Guest Lecturer, Villanova University Sustainability, Philadelphia.

Speaking engagements: Semiconductor Manufacturing

- 2007: Keynote Speaker, Willamette Valley National Engineers Week Banquet.
- 2005: Invited Speaker, Intel Technical Lecture Series, Carnegie Mellon University. "Innovations in Silicon Technology"
- 2005: Guest Lecturer, Materials Science and Engineering, Carnegie Mellon University. "Materials Science in Semiconductor Manufacturing"
- 2004: Invited Speaker, University of Oregon Graduate Women in Science Seminar. "Women in Technology"
- 2004: Invited Speaker, Center for Silicon System Implementation Seminar Series, Carnegie Mellon University. "Silicon Research at Intel"
- 2003: Invited Speaker, Hewlett-Packard Corporation. "Silicon Nanotechnology Research at Intel"
- 2003: Invited Speaker, University of Oregon Materials Science Institute Retreat. "Extending Moore's Law with Nanotechnology"

- 2003: Invited Speaker, Electrical and Computer Engineering Seminar Series, Carnegie Mellon University. "Nanotechnology in Semiconductor Manufacturing"

Leadership Summary

- Budget responsibility up of ~$25M annually. ~4300sq ft lab space across three geographies.
- Technical career advancement in Memory and IO technologies team (2017-present): 1 Intel Fellow, 3 Senior Principal Engineers, 2 Principal Engineers. Team of 80 filed 55 for new patents in 2019 and 180 submitted in prior years were granted.
- Team compositions included technicians through fellows, all degree levels, backgrounds Materials Science Engineering, Electrical Engineering, Computer Engineering, Mechanical Engineering, Chemical Engineering, Environmental Health and Safety, Finance, Communications, Business.
- Current team comprised of ~30% Technical female and/or underrepresented minorities.
- Contract negotiations of >$1B combined. (supply chain)
- Developed relationships with critical governmental and external organizations as needed to drive Intel programs forward, including environmental agencies within the US and China, The US State Department, Indonesian Ministry of Trade, the London Bullion Market Association, The World Gold Council, and leaders within the tin and gold industries.